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FULL ADDER CIRCUIT DESIGN WITH LOW POWER AND HIGH SPEED AT 0.25µM CMOS TECHNOLOGY USING TANNER EDA

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ABSTRACT

A CMOS Full Adder is designed using Tanner EDA Tool based on 0.25µm CMOS Technology. In the arithmetic logic unit (ALU), the full adder cell is one of the most frequently utilized digital circuit components and the fundamental functional unit of all computational circuits. Right now, a lot of work has been done to improve the architecture and functionality of full adder circuit designs. In this research, two innovative 1-bit full adder cell designs are developed using ten transistors and 0.25mm CMOS technology (10-T). Tanner software tools will be used in the design of the CMOS full adder to simulate the schematic and layout as well as compare the schematic and layout for the purpose of determining precise design limitations. As part of this, we are going to perform the simulation of the CMOS full adder using T-SPICE of Tanner EDA and its layout design using the Microwind tool. The parameters such as power consumption, Area, Propagation Delay, and Power Delay Product (PDP) are evaluated to analyze the proposed one-bit full adder.

Key words*: Low power, CMOS, Full Adder, EDA*

I.INTRODUCTION

Demand for the usage of battery-based portable electronic systems is increasing day by day; as the devices are portable they need batteries for driving them. So power consumption and speed become the main concern in designing of devices such as laptops, tablets, mobile phones, notebooks, and many other personal communication devices. Power consumption plays a vital role in VLSI technology. More power consumption leads to more heating which results in decreasing battery life and also needs a cooling fan to cool the circuitry. Therefore, power consumption affects the battery life and the cost of the whole system. Mostly all digital communication devices and the devices about which we have discussed above are used in the applications like digital signal processing, image and video processing, microcontrollers, and these applications use various arithmetic and logic operations to perform addition, subtraction, multiplication, etc. All these operations like addition subtraction and multiplication could be performed internally with the help of adder cells only [1]. Since a one-bit adder circuit (cell) plays the most important role in designing these digital communication devices, power consumption will be greatly decreased as well as the speed of operation also greatly increased [2]. Frequently all digital communication devices have multiple numbers of 1-bit full adder cells integrated within it to perform one or many bits' addition operations, this is the reason the adder cell plays an important role in determining the performance of the whole system. the proposed 1-bit adder cell designed with the help of CMOS XOR and CMOS XNOR circuits gives a better performance in terms of speed, Area, and power consumption.

II.RELATED WORKS

Till now in the digital world, different types of full adder cells are designed with different logic styles. Some of them are good for low power application, some of them for high speed, few of them full fill minimum area requirement but all these designs have their own merits and demerits. According to requirement of applications these adders are used. Few full adder cells which are already implemented are conventional (10T) full adder cells [3-6], Static Energy Recovery Full adder cells (SERF) [7-10], Gate Diffusion Input (GDI) full adder Cells [11, 12], etc. The Most complex computational circuit requires full adder circuitry hence the whole power consumption and speed of a computational circuit can be managed by implementing the low-power and high speed adder cell, so the overall performance of computational circuits totally depends on the adder cell. The ordinary C-CMOS 1-bit adder cell shown in Fig. 1 is based on a typical CMOS structure and uses 10 transistors. The high power consumption of the circuit is a result of the huge number of transistors utilized in its design, and the critical path with the circuit's input contains 5 transistors in its forward path, increasing the propagation delay [1-4, 6, 13]. The main benefit of this circuit is that it delivers the entire output voltage swing because this design does not employ complementary input signals, which reduces the short circuit current, thus this circuit has a high noise margin which is why it is reliable to operate at low voltages.

III. PROPOSED SYSTEM

After doing an analysis of all existing full adder cells two new designs have been proposed, which are implemented with the help of ten transistors. The first proposed circuit is implemented by using the XOR module shown in Fig.1, it uses two XOR module sections and one inverter section. Each XOR module is made by using 4 CMOS transistors (2 NMOS & 2 PMOS). The only difference between the first and second proposed adder cells is that the second adder cell is made with the help of two XNOR modules instead of using two XOR modules. These two proposed circuits are giving better power and delay as compared with the existing 10T structure i.e. SERF and GDI. The problem with SERF and GDI one-bit full adder is output voltage swing which is also present in the proposed 1-bit adder cell but it has better performance (less delay), lesser power consumption, and efficiently less power delay product.

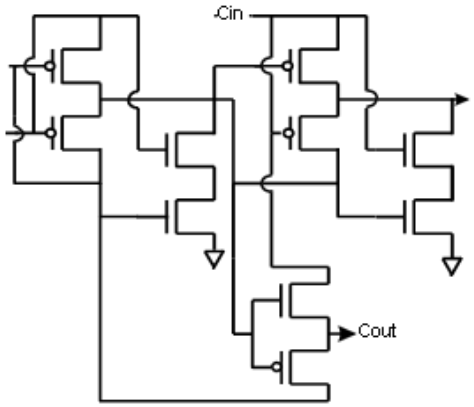

Fig.1 Proposed full adder cell using XOR module

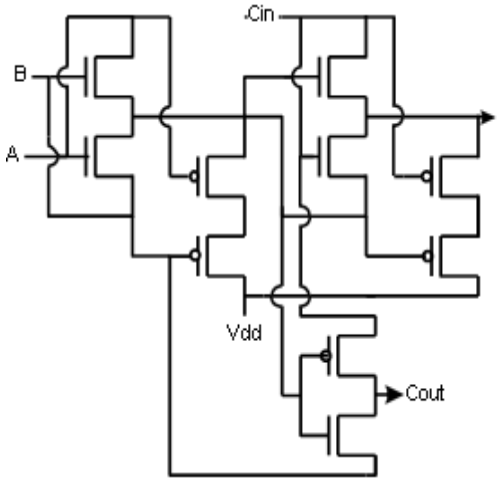

Fig.2. Proposed full adder cell using XNOR module

The schematic of the proposed full adder designed using XNOR, which requires 10 Transistors, is shown in fig.2. The body biasing profile of all the NMOS transistors is the same, where the substrate is connected to the zero potential, i.e. ground. While the body biasing profile for PMOS is that the substrate is connected to the voltage supply, i.e. Vdd. This body biasing profile is adopted as it contributes to the reduction of leakage power of a circuit. The proposed full adder in 180nm technology has a length equal to 180nm for all the transistors and the width of the transistors Tn1 and Tn2 is 540nm while for the remaining transistors, it is 240nm. Whereas for the 65-nm technology, the length is 65nm and the width of Tn1 and Tn2 is 150nm while for the remaining transistors, it is 80nm.

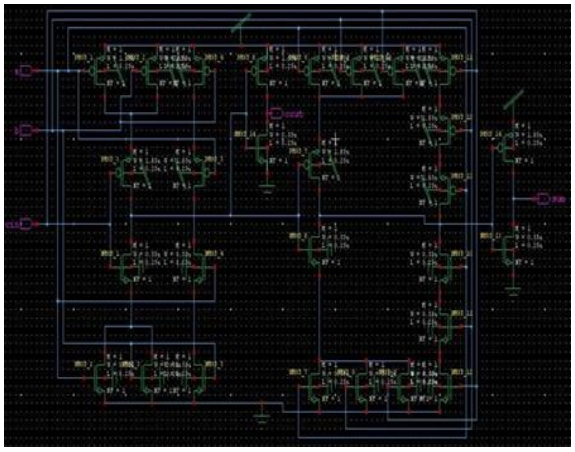

Fig 3: Schematic Diagram of 10T Full adder

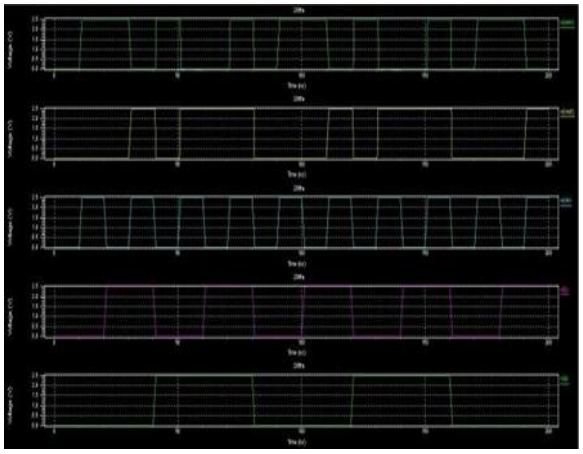

Fig 4: Schematic Wave Form of 10T Full adder

VI.CONCLUSION

The project demonstrates the design and execution of a CMOS Full Adder based on 0.25-m CMOS technology utilizing the Tanner EDA Tool. Tanner software tools are used to simulate the schematic and layout as well as compare the schematic and layout of a CMOS full adder during design, which aids in determining precise design limitations. According to the simulation results it is observed that the proposed designs have achieved a maximum saving of power and maximum reduction in delay and maximum saving of PDP, when compared to the existing SERF and GDI adder respectively. The proposed circuits are also giving better performance at different supply voltage compared to existing adder circuits.

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